PROCESSING SYSTEM HAVING SEQUENTIAL ADDRESS INDICATOR SIGNALS

Abstract of the Disclosure

Embodiments of the present inventions relate to processors having sequential address indicator signals, also referred to as sequence signals, for indicating when accessed addresses are sequential. One embodiment relates to a processing system for accessing memory having an address bus for providing a current address and a previous address to memory, a data bus, an execution unit, and a decode control unit. The processing system further includes a fetch unit, coupled to the execution unit, the decode control unit, the address bus, and the data bus, for generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address.